Amendments to the specification

Please replace paragraph 2 on page 1 with the following revised paragraph:

This application is related to the following copending applications, all of which are incorporated herein by reference: Serial No. 09/996,113, filed November 28, 2001, for "Unified Digital Architecture[["]]" (Docket No. RAL920010003US2); Serial No. 09/996,091, filed November 28, 2001, for "Architecture for Advanced Serial Link Between Two Cards" (Docket No. RAL920010004US2); and Serial No. 09,996,053, filed November 28, 2001, for "Analog Unidirectional Serial Link Architecture" (Docket No. RAL920010005US2).

Please replace paragraph 3 on page 12 with the following revised paragraph:

The data path includes ~~of a~~ shift register 250 which loads two bits from the data correlation blocks during each half-rate cycle. The shift register is loaded to a word data register 252 (8 or 10 bits) using a word clock derived from the PLL clock. A rate counter 254 controls the shift register 250 and the 8/10 bit register 252.